400Gb/s QSFP-DD SR8 100m Transceiver
HXEX-MM1R2C

Features

- Up to 53.13Gb/s data rate per lane and 425Gb/s aggregate bit rate
- 8x53Gbps PAM4 transmitter and PAM4 receiver
- 8 channels 850nm VCSEL array and 8 channels PIN photo detector array
- Maximum link length of 70m on OM3 MMF and 100m on OM4 MMF
- MPO-16 optical cable connection
- QSFP-DD mechanical specification compliant with QSFP-DD MSA
- Compliant with IEEE 802.3bs400GAUI-8 standard
- Compliant with CMIS 4.0
- Operating case temperature 0°C~70°C
- 3.3V single power supply
- power dissipation <10W
- Compliant with RoHS 2.0Case operating temperature
  Commercial: 0 ~ +70°C

plications

Data Center
400GBASE-SR8 400G Ethernet

Part Number Ordering Information

Part Number	Data Rate (Gb/s)	Wavelength (nm)	Transmission Distance(m)	Temperature (°C) (Operating Case)
HXEX-MM1R2C	425	850	100	0~70 commercial

I. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T_S	-40	85	°C	
Power Supply Voltage	V_{CC}	-0.3	3.6	V	
Relative Humidity (non-condensation)	RH	5	95	%	
Damage Threshold	TH_d		5.0	dBm	

II. Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	T_{OP}	0		70	°C	commercial
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate				425	Gb/s	
Control Input Voltage High		2		Vcc	V	
Control Input Voltage Low		0		0.8	V	
Link Distance (MMF)	D			70	m	OM3
				100	m	OM4

III. General Description

Walsun'400G QSFP-DD SR8 optical transmitter is an Eight-Channel, Pluggable, Parallel, Fiber-Optic QSFP Double Density for 2x200 Gigabit Ethernet Applications. This transceiver is a high-performance module for short-range multi-lane data communication and interconnection applications. It integrates eight data lanes in each direction with 8x26.5625GBd. Each lane can operate at 53.125Gbps up to 70 m using OM3 fiber or 100 m using OM4 fiber with FEC. These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 76 contact edge type connector. The optical interface uses a 16 fiber MTP (MPO) connector. The Common Management Interface Specification (CMIS) for QSFP DD modules, this module incorporates Gigalight Technologies proven circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

IV. Pin Assignment and Pin Description

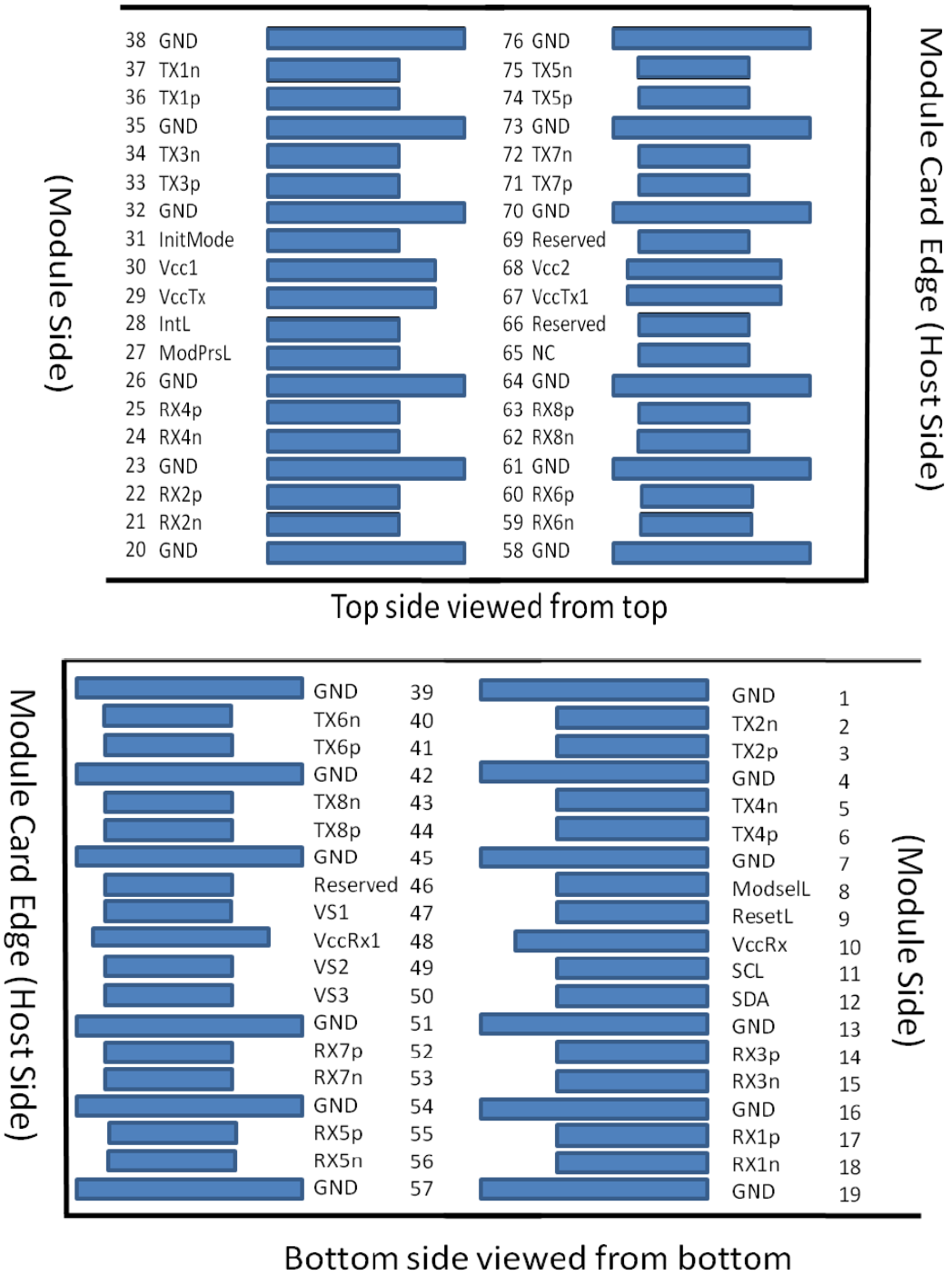

Figure1. Diagram of host board connector block pin numbers and names

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	TWI serial interface clock	3B	
12	LVCMOS-I/O	SDA	TWI serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode/ TxDis	Low Power mode/optional TX Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
46	LVCMOS /CML-I	P/VS4	Programmable/Module Vendor Specific 4	3A	5
47	LVCMOS /CML-I	P/VS1	Programmable/Module Vendor Specific 1	3A	5
48		VccRx1	3.3V Power Supply	2A	2
49	LVCMOS /CML-O	P/VS2	Programmable/Module Vendor Specific 2	3A	5
50	LVCMOS /CML-O	P/VS3	Programmable/Module Vendor Specific 3	3A	5
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	3A	6
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a steady state current of 500 mA.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 1500 mA.

3. Reserved and no Connect pads recommended to be terminated with 10 k to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module.

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

5. Full definitions of the P/VSx signals currently under development. On new designs not used P/VSx signals are recommended to be terminated on the host with 10 k.

6. ePPS/Clock if not used recommended to be terminated with 50 to ground on the host.

V. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Power Consumption	p			10.0	W	
Supply Current	Icc			3.1	A	
Data Rate, Each Lane			26.6125		GBd	PAM4
Input Differential Impedance	Zin	90	100	110	Ω	
Output Differential Impedance	Zout	90	100	110	Ω	
Differential Input voltage	Vppin	200		900	mV	
Differential Output Voltage	Vppout	200	-	900	mV	

VI. Optical Characteristics

The following optical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Transmitter						
Lane wavelength（range）	λC	840	850	860	nm	
Optical Spectral Width	Δλ			0.6	nm	
Average Launch Power each lane	PAVG	-6.5		4	dBm	
Optical Modulation Power (OMA), each Lane	OMAouter	-4.5		3	dBm	1
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	TDECQ			4.9	dB	
Optical Extinction Ratio	ER	3			dB	
RIN OMA				-128	dB/HZ	
TX OFF Output Power	Poff			-30	dBm	

Receiver						
Center Wavelength	λ_C	840		860	nm	
Average receive Power, each lane		-8.4	-	4	dBm	
Receive power (OMAouter), each lane		-	-	3	dBm	
Damage Threshold	Pmax	5	-	-	dBm	
Receiver sensitivity (OMAouter), each lane		RS=max（-6.5,SECQ-7.9）			dBm	1
Stressed receiver sensitivity	SEN	-	-	-3.4	dBm	
LOS De-Assert	LOSD	-	-	-12	dBm	
LOS Assert	LOSA	-30	-		dBm	
LOS Hysteresis	LOSH	0.5	-		dB	

Notes:

1. For BER=2.4E-4 Pre-FEC

VII. Mechanical Dimensions

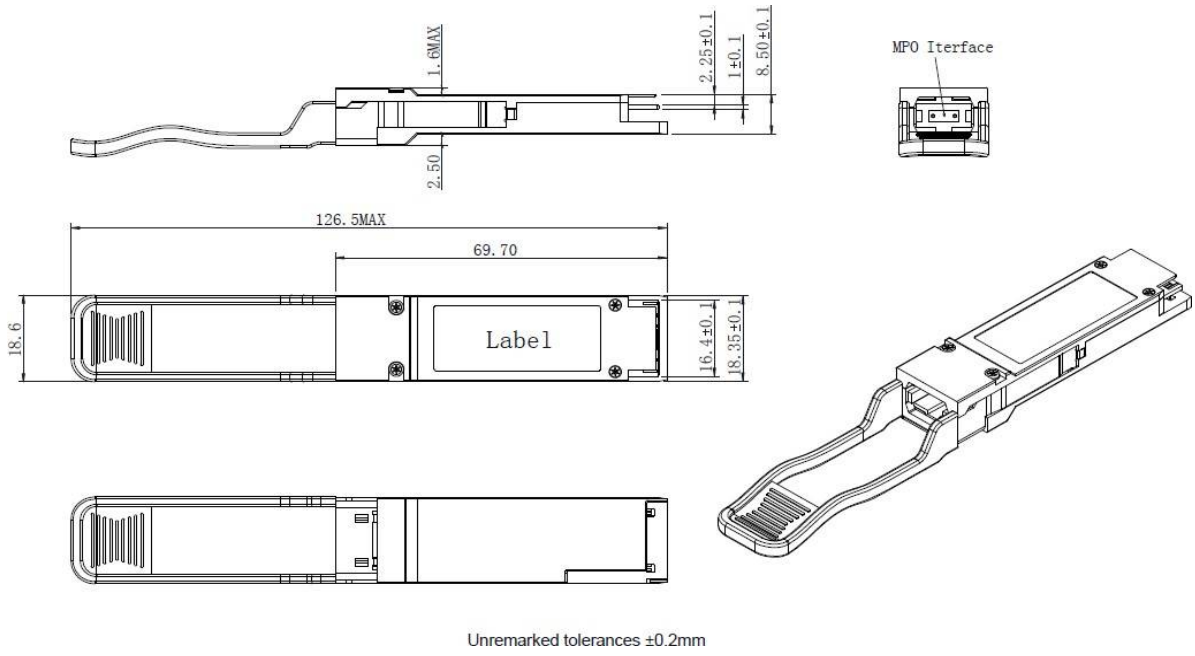

Figure2. Mechanical Outline

VIII. Revision History

Version No.	Initiated	Revised contents	Release Date
V1.0	Andy Zhang	Preliminary datasheet	2023-09-20

IX. Contact us

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